Hardware Modelling

Exercise

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Task Description (1)

- Simple calculator with following operations:
  - Addition
  - Subtraction
  - Multiplication
  - Division
- I/O
  - PS/2 keyboad
  - VGA monitor
- History memory for last computations
  - Uploadable to PC (RS232)

Task Description (2)

- Arithmetic expressions

```
DIGIT  = "0" | "1" | "2" | "3" | "4" | "5" | "6" | "7" | "8" | "9" ;
UNSIGNED = DIGIT { DIGIT } ;
OPERAND = ["-"] UNSIGNED ;
OPERATOR = "+" | "-" | "*" | "/" ;
EXPRESSION = OPERAND { OPERATOR OPERAND } ;
```

- Operator precedence:
  1. Mult, Div
  2. Add, Sub
- Example: 180 + 6 / -3 – 139 + 3
  - Result: 42
- Data type: signed long (-2^{31} to $2^{31} - 1$)

Task Description (3)

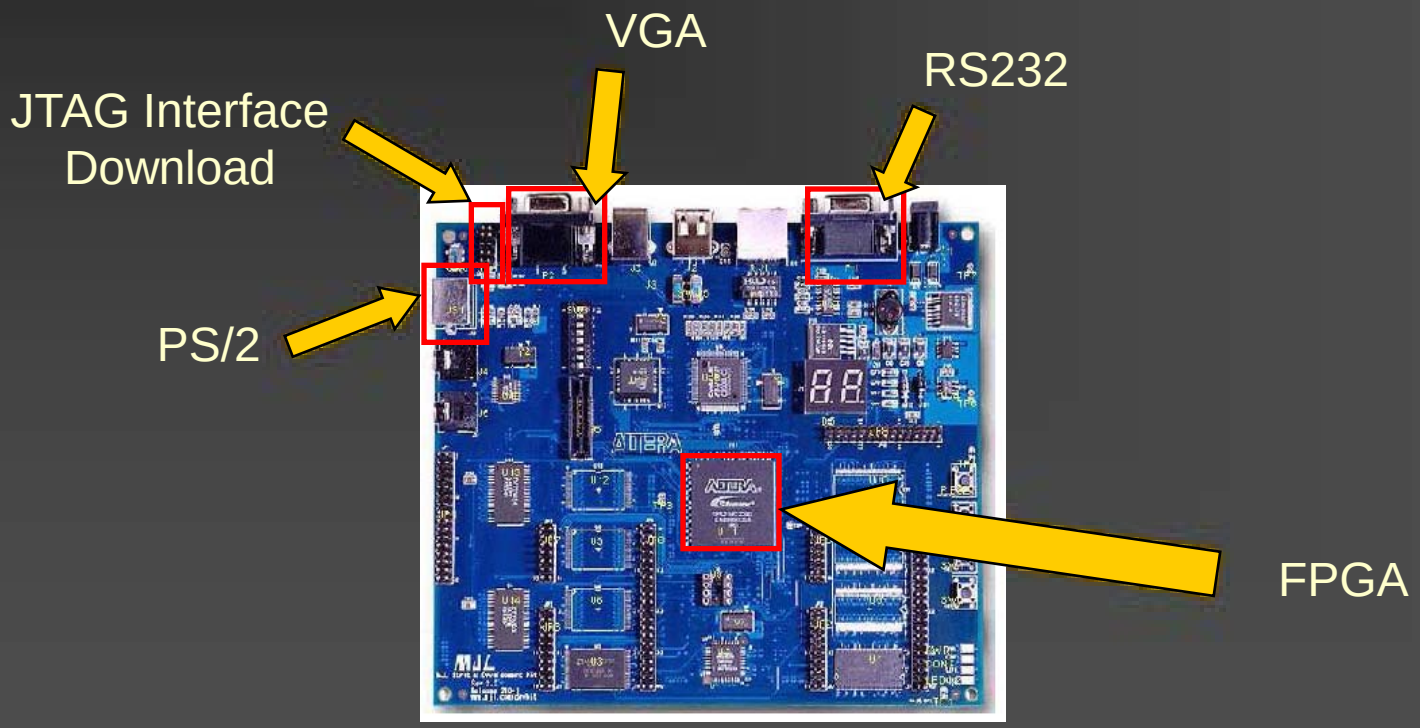
- Input of arithmetic expressions
  - Displayed in one line on the monitor
    - Up to 70 characters long
  - Space characters should be shown on screen
  - Hitting backspace deletes last character
  - Hitting <Enter> starts the computation
    - Output result on screen (e.g. in next line)
    - Goto new empty line for next input
- Available components
  - PS/2 interface (VHDL)
  - VGA interface (VHDL)

Task Description (4)

- Buffer for last computations
  - Store arithmentic expressions & results
  - Buffer depth: last 50 computations
  - Send memory content to PC
    - Via RS232: e.g. 8N1, baudrate 115.200
    - Initiate transfer: when key pressed on development board, when requested from serial interface
- RS232 interface must be implemented by yourself (don't use third-party cores)

Target Platform

- Rapid Prototyping Board wit an Altera Stratix FPGA (same board used in „Digital Design Lab“)



Schedule (I)

- Write a design document
  - High-level design description
  - Detailed design description
  - Submission deadline: Fri, 26.03. 23:59 (via MyTI)
- Peer-Review
  - Evaluate the document of two other groups
  - Submission deadline: Fri, 16.04. 23:59 (via MyTI)
- Final submission of the design document
  - Submission deadline: Fri, 30.04. 23:59 (via MyTI)

Schedule (II)

- Implementation
  - VHDL Entry / Simulation / Synthesis / Hardware Testing
  - Submission deadline: Fri, 28.05. 23:59 (via MyTI)
- Weekly Q&A hours:
  - Mo, 14:00-15:00
  - Wed, 10:00-11:00
  - Before March 26: At the institute (Treitlstraße, 2nd floor)
  - After March 26: In the lab room

Specification

- High-level design description
  - Requirement specification
  - Decomposition in submodules (schematic)
  - Interface definition
  - Testcase specification
- Detailed design description
  - Implementation description of a submodule

External Interfaces (1)

- Physical Interfaces
  - Interface to key pad
  - Interfaces to VGA, PS/2, RS232
  - Reset und Clock!
  - Active Low oder Active High
  - …
- Logical Interfaces
  - How to control the VGA component
  - How to read the keyboard input
  - …

External Interfaces (2)

- Behavioural Interface
  - Allowed keyboard input
  - What about overflows?
  - Erroneous inputs
  - Output on the screen
  - Error messages
  - …

Detailed design description

- Description how the design will be implemented
- Event sequence digrams
- Internal structure
  - Memory
  - Logic blocks
  - Parallel processes
  - State machines

Testcases

- Example for testcases
  - TC1: adding two positive numbers – covers requirement 1,3,6
  - TC2: erroneous input (too large numbers, …) - covers requirement 2,7
  - TC3: …

⇒ All requirement have to be covered by testcases

Deliverables - Specification

- Length: approx. 10 pages
- Upload as PDF on the TI Portal
- First version: blinded for review, i.e., no author names, no group numbers
- Final version: Title page with author names