MJL Stratix Development Board

December 2002, ver. 1.0 Data Sheet

Introduction

This data sheet describes the features and functionality of the MJL Stratix Development board.

Development Board Features

- Stratix ™ EP1S25 device
- 4 Mbyte (4Mbit x 8-bit/2Mbit x 16-bit) of flash memory
  - Can be ordered with 4 -16MB of flash
  - pre-configured with the 32-bit Nios reference design and software
- 256 Kbytes of SRAM (in two 64 K x 16-bit chips)
- 8 Mbytes of SDRAM(512K x 32 x 4 banks)
  - Can be ordered with 8-32MB of SDRAM
- On-board logic for configuring Stratix device from flash memory
- 3.3-V expansion/prototype headers (access to 40 user I/Os)
- 5-V-tolerant expansion/prototype headers (access to 40 user I/Os)
- One RS-232 serial connector
- One SL811HS Embedded USB Host/Slave Controller
- Keyboard/Mouse port (PS/2)
- VGA port
- AD733llL A/D, D/A Converter
- One user-definable 8-bit DIP switch block
- Two user-definable push-button switches
- Reset, and clear push-button switches
- Dual 7-segment LED display
- Two user-controllable LEDs
- Joint test action group (JTAG) connector for ByteBlasterMV™ and MasterBlaster TM download cables
- One Mictor Connector
- Oscillator and zero-skew clock distribution circuitry
- Additional socket for a user selected oscillator.
- Power-on reset circuitry
- Power-supply circuitry (Input: 9-V unregulated, center-negative)

Functional Overview

The Stratix development board provides a hardware platform to immediately start developing embedded systems based on Altera ®Stratix TM devices. The Stratix development board is pre-loaded with a 32-bit Nios embedded processor system reference design. A Quartus® II project directory containing the reference design example is installed with the Nios development software. The reference design

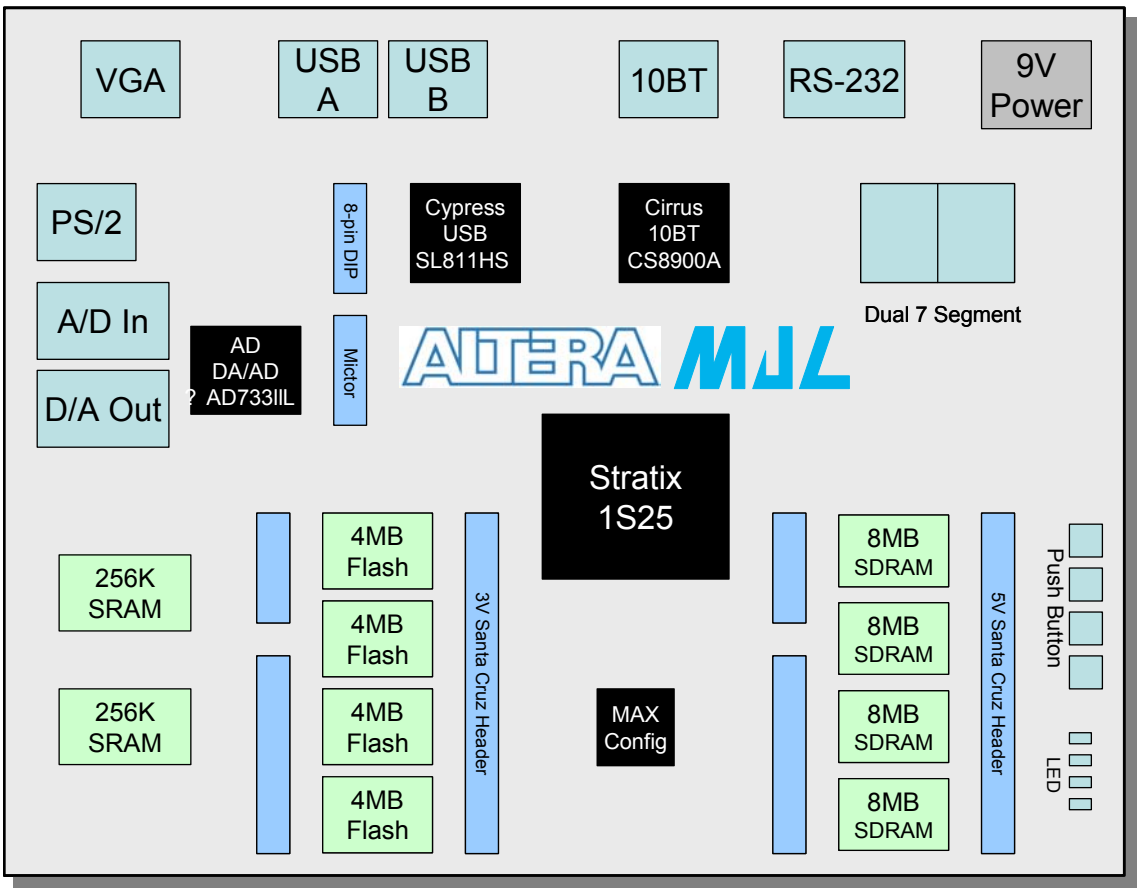
and software
are pre-loaded in flash memory, and boot on power-up. The reference design software includes a monitor that can be used to download and debug programs, running examples to all of the interfaces on the board (memory, USB, Ethernet, UART, A/D & D/A converters, PS/2, VGA, etc., as well as a sample Tetris game).

Stratix Development Board Components

This section contains a brief overview of several important components on the Stratix development board. A more complete list of components appears in Table 2 on page 20. A complete set of schematics, a physical layout database, and GERBER files for the Stratix development board are installed as documentation .

Choose **Start > Programs > Altera > Excalibur > Nios Documentation** (Windows Start menu) for board-related files.

Figure 1. MJL Stratix Development Board Block Diagram



The Stratix EP1S25F672 Device

U11 is an Stratix EP1S25F672 device in a 672-pin FineLine BGA™ package. A useful Nios system module (CPU and peripherals) typically occupies between 25% and 35% of the logic on this device.

Table 1. Stratix EP1S25F672 Device Features	
Maximum system gates	8,400,000
Typical gates	650,000
Les	25,660
Maximum RAM bits	1,944,576
Maximum user I/O pins	469

The development board provides two separate methods for configuring the Stratix device:

1. A JTAG connection (JP9) that can be used with Quartus II software via a ByteBlasterMV or MasterBlaster download cable.
2. A configuration controller (U2) that configures the Stratix device at power-up from hexout files stored in the flash memory (U3). See “Configuration Controller” on page 14 for more information.

Flash Memory Chip

U3, U6, U9, and U17 are Advanced Micro Devices (AMD) AM29DL323D 4 Mbyte flash memory chips. One flash memory device is included on the board, and room for at most four-4Mbyte memories, for a total of 16MB of flash. The flash memory is connected to the Stratix device so that it can be used for two purposes:
The Stratix device can use the flash as general-purpose readable, memory and non-volatile storage.
The flash memory can hold a Stratix device configuration file that is used by the configuration controller to load the Stratix device at power-up. See “Configuration Controller” on page 15 for related information.

A hexout configuration file that implements the 32-bit Stratix reference design is pre-loaded in this flash memory. The 32-bit reference design, once loaded, can identify the 4 Mbyte flash in its address space, and includes monitor software that can download files (either new Stratix device configurations, Nios software, or both) into flash memory. The Nios software includes subroutines for writing and erasing this specific type of AMD flash memory.

Dual SRAM Chips

U4 and U13 are 256 Kbyte (64 K x 16-bit) asynchronous SRAM chips. They are connected to the Statix device so they can be used by a Nios processor as general-purpose zero-wait-state memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The pre-loaded Stratix reference design identifies these SRAM chips in its address space as a contiguous 256 Kbyte, 32-bit-

wide, zero-wait-state main memory.

SDRAM

U1, U5, U7, and U10 are Micron (MT48LC2M32B2TG-7) 64Mbit SDRAM devices. The SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 2,048 rows by 256 columns by 32 bits. One SDRAM memory device is included on the board, and room for at most four 64Mbit memories, for a total of 32MB of SDRAM.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access. The preloaded reference design utilizes the SDRAM controller included in the Quartus II software to access the memory.

Expansion Prototype Connector

Headers JP2, JP4, and JP5 collectively form a standard-footprint, mechanically-stable connection that can be used (for example) as an interface to a special-function daughter card. Contact your Altera sales representative for a list of available expansion daughter cards that can be used with the Stratix board.

The 3.3-V expansion prototype connector interface includes:

- 40 Stratix device general-purpose I/O signals.
- A buffered, zero-skew copy of the on-board OSC output (from Y1).
- A buffered, zero-skew copy of the Stratix's phase-locked loop (PLL)-output (from Y1).
- A Stratix device clock-input (for daughter cards that drive a clock to the programmable logic device (PLD).
- A logic-negative power-on-reset signal.
- Two regulated 3.3-V power-supply pins (500 mA total max load).
- Unregulated power-supply pin (connects directly to J1 power-input plug).
- Numerous ground connections.

Figure 2. 3.3-V Expansion Prototype Connector – JP4

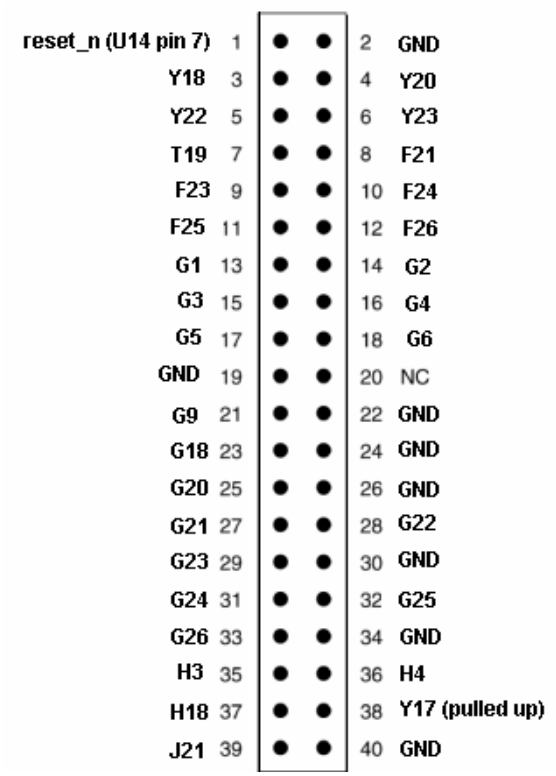
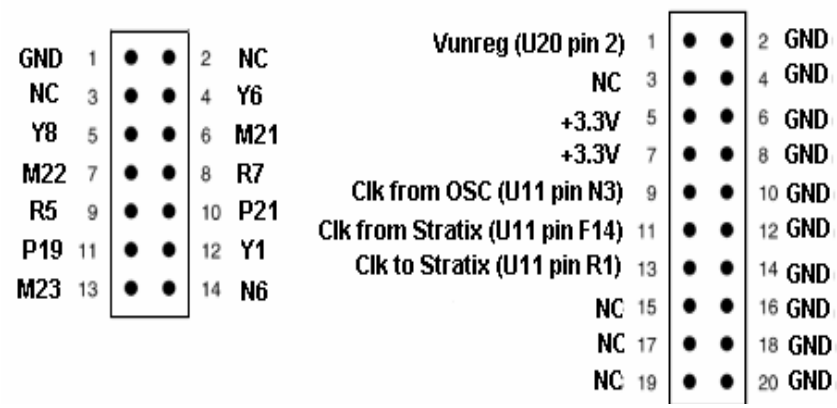


Figure 3. 3.3-V Expansion Prototype Connector – JP2, JP5



Expansion Prototype Connector Header: 5-V tolerant.

Headers JP3, JP6, and JP7 collectively form a standard-footprint, mechanically-stable connection that can be used (for example) as an interface to a special-function daughter card. The 5-V-tolerant expansion connector is similar to the 3.3-V expansion connector, except as indicated herein below:

- JP6 (pin 38) is used as a global card-enable signal. These analog switches are globally enabled (switched-on) by Stratix device I/O pin M20 (logic-0 on M20 enables switches).
- A low-current 5-V power supply (50 mA max load) is presented on pin 2 of JP7 (the corresponding pin on the 3.3-V expansion connector is not connected).
- An RC-filtered connection to Stratix device I/O pin (Y10). This circuit is suitable for producing a high-impedance, low-precision analog output if Y10 is driven with a duty-cycle-modulated waveform by user-logic. The corresponding pin on the 3.3-V expansion connector is not connected.
- The Vref-voltage for the analog switches (3.3-V plus one diode-drop) is presented on pin 3 of JP3. The corresponding pin on the 3.3-V expansion connector is not connected.

Figure 4. 5V Expansion Prototype Connector – JP6

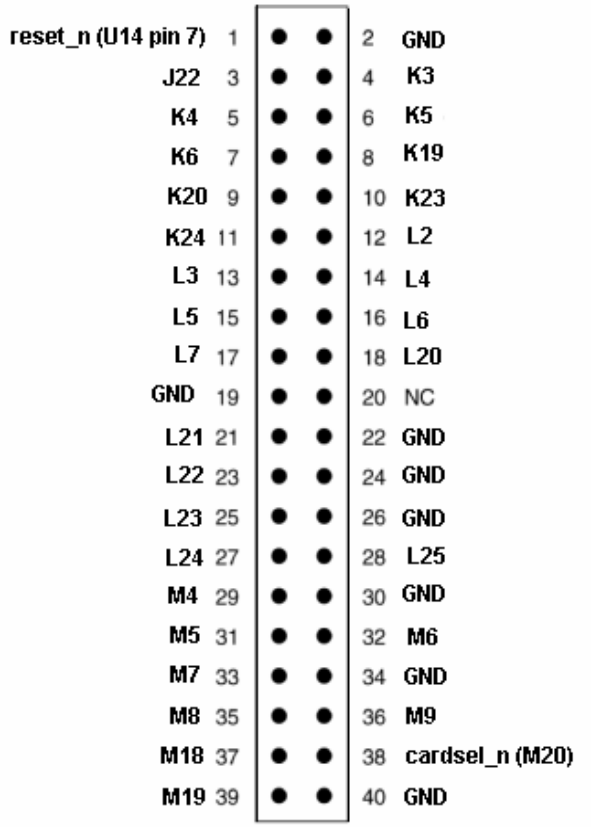
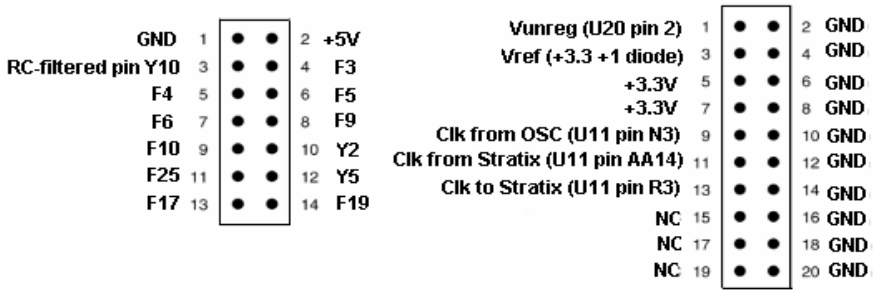


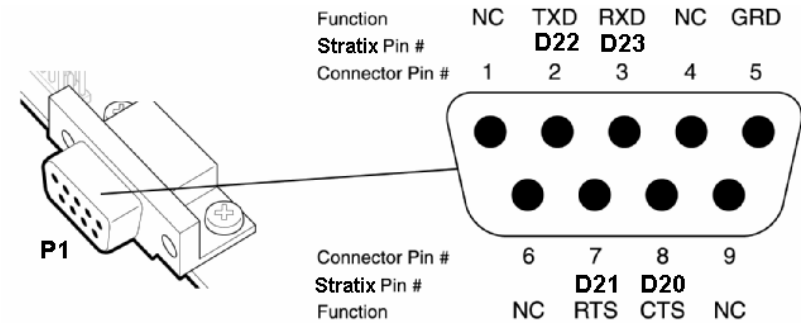
Figure 5. 3.3-V Expansion Prototype Connector – JP3, JP7



Serial Port Connector

P1 is a standard DB-9 serial connector. This connector is typically used for host communication with a desktop workstation. Using a standard 9-pin serial cable connected to (for example) a COM-port. The transmit (TXD) from Nios, receive (RXD) by Nios, clear to send (CTS) and ready to send (RTS) signals use standard high-voltage RS-232 logic levels. U9 is a level-shifting buffer that presents or accepts 3.3-V versions of these signals to and from the Stratix device.
Figure 6 shows the pinout information on a design using a single UART with hardware handshaking.

Figure 6. Serial Port Connector



AD73311L AD/DA Converter

U15 is Analog Device AD73311L 16-bit AD/DA converter. It provides a 16-bit A/D conversion channel, a 16-bit D/A conversion channel, and a powered output. Sample code for the control functionality of the AD/DA converter is included on the CD. The AD/DA converter is accessable by 2 minijacks. A microphone (or equivilant analog signal) can be connected to the A/D channel through J4. J5 minijack provides a powered output from the D/A channel of the device. Maximum output power from this channel is 33mW at 2.7V (typical headphone or powered speaker). Do not connect a non-powered speaker or other device that will exceed the maximum power ouput of the D/A connection.
The AD73311L is a complete front-end processor for general purpose applications including music, speech, and telephony. It features a 16-bit A/D conversion channel and a 16-bit D/A conversion channel. Each channel provides 70 dB signal-to-noise ratio over a voiceband signal bandwidth. The final channel bandwidth can be reduced, and signal-to-noise ratio improved, by external digital filtering in a DSP engine. The AD73311L is suitable for a variety of applications in the speech and telephony area, including low bit rate, high quality compression, speech enhancement, recognition and synthesis.

The gains of the A/D and D/A conversion channels are programmable over 38 dB and 21 dB ranges respectively. An on-chip reference voltage is included to allow single supply operation.

- 16-Bit D/A Converter
- 16-Bit A/D Converter
- Programmable Input/Output Sample Rates
- 76 dB ADC SNR
- 77 dB DAC SNR
- Programmable Sampling Rate
- Programmable Input/Output Gain
- Single (+3 V)Supply Operation
- 33 mW Max Power Consumption at 2.7 V
- General Purpose Analog I/O

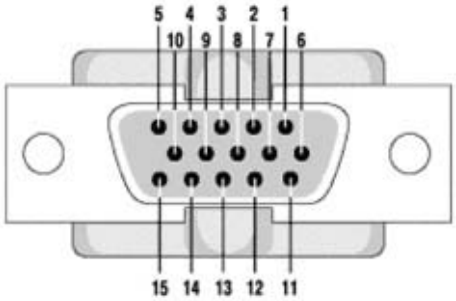
VGA Interface

P2 is 15-pins VGA Connector which can be connected to the monitor. The VGA connector allows the Stratix EP1S25F672 device to control an external video monitor. The VGA Monitor accepts three analog signals in the range of 0 to 0.7V. Using a few more registers VGA output can be easily produced.

Information about the color of the screen, and the row and column indexing of the screen, are sent from the Stratix EP1S25F672 device to the monitor via five signals. Three VGA signals are red, green, blue, while the other two signals are horizontal and vertical synchronization. Manipulating these signals allows images to be written to the monitor's screen.

Sample control firmware, and a simple tetris game are included for reference.

Figure 7. VGA Connector

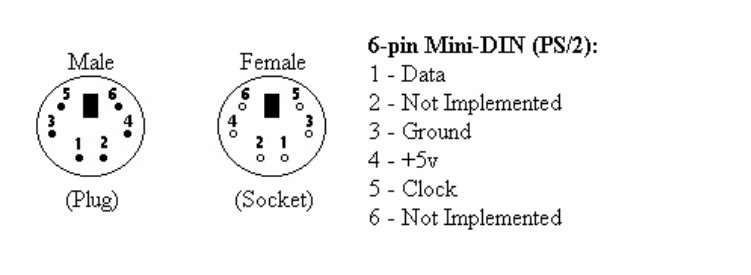


Pin	Signal	Pin	Signal
1	Red Drive	9	Plug
2	Green Drive	10	Ground
3	Blue Drive	11	Monitor Sense 0
4	Reserved	12	Monitor Sense 1
5	Ground	13	Horizontal Sync
6	Red Ground	14	Vertical Sync
7	Green Ground	15	Reserved
8	Blue Ground		

PS2 Keyboard /Mouse Connector

JS1 is PS2 connector which can be connected to mouse or keyboard. The mouse interface, which consists of a 6-pin mini-DIN connector, allows the Stratix EP1S25F672 device to receive data from a PS/2 mouse or a PS/2 keyboard. The Stratix develop board provides power and ground to the attached mouse or keyboard. The Stratix EP1S25F672 device input and output the DATA_CLOCK signal to the mouse and inputs the data signal from the mouse.

Figure 8. PS2 Connector



Ethernet Interface Card

U16 is Cirrus logic CS8900A Ethernet controller and RJ1 is RJ45 port for cable connection. The Ethernet interface card allows the Stratix EP1S25F672 device to control an Ehternet controller. In the development board, the Cirrus Logic CS8900A Ethernet controller is capable of communicated with Ethernet peripherials.

The CS8900A is a low-cost Ethernet LAN Controller optimized for Industry Standard Architecture (ISA) personal computers. Its highly-integrated design eliminates the need for costly external components required by other Ethernet controllers. The CS8900A includes on-chip RAM, 10Base-T transmit and receive filters, and a direct ISA-Bus interface with 24 mA Drivers.

In addition to high integration, the CS8900A offers a broad range of performance features and configuration options. Its unique PacketPage architecture automatically adapts to changing network traffic patterns and available system resources. The result is increased system efficiency.

The CS8900A is available in a 100-pin TQFP package ideally suited for small form-factor, cost-sensitive Ethernet applications. With the CS8900A, system engineers can design a complete Ethernet circuit that occupies less than 1.5 square inches (10 sq. cm) of board space

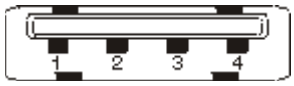
- single-chip IEEE 802.3 Ethernet solution
- Full duplex operation
- On-chip RAM buffers transmit and receive frames
- 10Base-T port and filters (polarity detection/correction)
- AUI Port for 10Base2, 10Base5, and 10Base-F
- LED drivers for link status and LAN activity
- A CS8900A integrated Ethernet 10Mbit PHY/MAC chip
- See http://www.cirruslogic.com/design/products/overview/detail.cfm?d=46 for more information about the CS8900A chip
- A RJ-45 network connector with integrated-transformer magnetics and Link/LAN LEDs
- A 20 MHz crystal oscillator that is used by the CS8900A chip
- All necessary resistors and capacitors

USB Connector

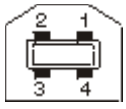
U17 is Cypress SL811HS USB Host/Slave Controller. J2 and J3 are ports for the connection of USB cable. The USB interface allows the Stratix EP1S25F672 device to control a USB 1.1 host/slave controller. If SW5 and SW4 go to “H”, it works as host. In the development board, the Cypress SL811HS USB Host/Slave Controller is capable of communicating with either full-speed (12Mbps) or low-speed (1.5Mbps)USB peripherals.

The SL811HS USB Host/Slave Controller incorporates USB Serial Interface functionality along with internal full-/low-speed trans-ceivers. The SL811HS supports and operates in USB full-speed mode at 12 Mbps, or at low-speed 1.5-Mbps mode and conforms to USB Specification 1.1.

Figure 9. USB Connector



Type A



Type B

JTAG Connector

JP9 is a 10-pin JTAG interface connector compatible with Altera ByteBlasterMV and MasterBlaster download cables. The JTAG connection can be used for any of two purposes:

1. Quartus II software can configure the Stratix EP1S25F672 device (U11) with a new bitstream (such as .sof) file via a MasterBlaster or ByteBlasterMV download cable.
2. Quartus II or MAX+PLUS ® II software can re-program the EPM3064 device (U2) with a new .pof file via a MasterBlaster or ByteBlasterMV download cable.

The JTAG chain on the Stratix development board can include all, some, or none of the following devices, in order:

1. The Stratix EP1S25F672 device (U11): SW6 switch should be set to “S”
2. The EPM3064 configuration controller (U2): SW6 switch should be set to “M”

The JTAG connection is most commonly used to download user configuration (such as .sof) files to the Stratix EP1S25F672 device during logic development and debugging.

The EPM3064 device (U2) comes factory-programmed as a configuration controller. MAX+PLUS II projects that include the design, implementation, and programming files for the configuration-controller logic are included with the Nios embedded processor software. Most users will never need to re-program the configuration controller (U2).

Configuration Controller

The configuration controller (U2), is an Altera EPM3064 PLD. It comes factory-programmed with logic that configures the Stratix EP1S25F672 device (U11) from data stored in flash (U3) on power-up. At power-up (or when the RESET switch is pressed), the configuration controller begins reading data out of the flash memory. The flash memory, Stratix device, and configuration controller are connected so that data from the flash configures the Stratix EP1S25F672 device in passive-parallel mode.

Configuration Data

The Quartus II software can (optionally) produce hexout configuration files that are directly suitable for download and storage in the flash memory as configuration data. A hexout configuration file for the

Stratix EP1S25F672 device (U11) is a little less than 1 Mbytes, and thus occupies about 1/4 of the flash memory (U3).

New hexout files can be stored in the flash memory (U3) by software running on a Nios processor. The preloaded 32-bit Nios reference design includes the GERMS monitor program, which supports downloading hexout files from a host (such as desktop workstation) into flash memory.

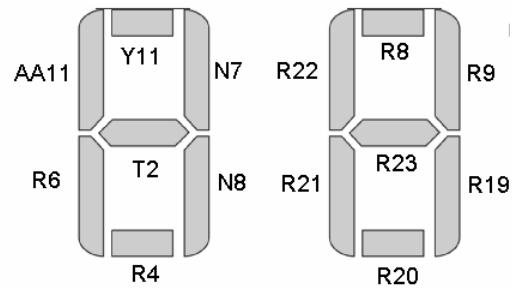
- See the Nios Embedded Processor Software Development Reference Manual for a detailed description of the GERMS monitor program.

A user can replace configuration data in flash memory to other reference design and download default configuration data (~\altera\excalibur\sopc_builder_2_5\examples\ full_peripherals_32.flash) if it is needed.

Two-Digit 7-segment display

D3 is connected to the Stratix device so that each segment is individually controlled by a general-purpose I/O pin.

Figure 10. Dual-Digit Display

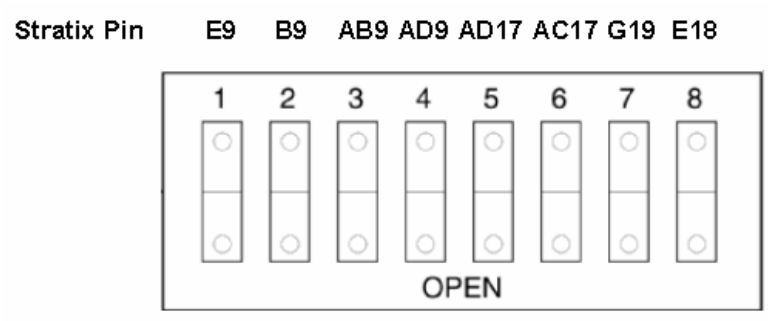


The pre-loaded Stratix reference design includes parallel input/output (PIO) registers and logic for driving this display. (Decimals in the above 7-segment display are not functional.)

Switches, Buttons, and LEDs

SW3 is an 8-DIP-switch block with each switch connected to an Stratix general-purpose I/O and a pull-up resistor. The Stratix device will see a logic-1 when each switch is open, and a logic-0 when each switch is closed.

Figure 11. Eight Dip Switch Block



SW1, and SW2 are momentary-contact push-button switches, each connected to an Stratix device general-purpose I/O and a pull-up resistor. The Stratix device will see a logic-0 when each switch is pressed. Discrete LEDs LED1 and LED2 are each controlled by the Stratix device general-purpose I/O. Each LED will light-up when the Stratix device drives a logic-1 on its controlling output.

The Stratix development board uses dedicated switches RESET and CLEAR for the following fixed functions:

RESET

When RESET is pressed, a logic-0 value is driven to U14, the power-on reset controller. Pressing RESET is equivalent to a power-on reset. When RESET is pressed (or when the board is power-cycled), the configuration controller will load the Stratix device from flash memory. See “Configuration Controller” on page 15 for more information. When the development board is delivered from the factory, the Stratix EP1S25F672 device will be configured with the 32-bit reference design at power-up (or when RESET is pressed). The reference design will then begin executing the GERMS monitor, a serial debug/download utility.

CLEAR

When CLEAR is pressed, a logic-0 is driven onto the Stratix devices'

DEV_CLRn pin (and user I/O F12). The result of pressing CLEAR depends on how the Stratix device is currently configured.

The pre-loaded Nios reference design treats CLEAR as a CPU-reset pin: The reference Nios CPU will reset and start executing code from its boot-address (0) when CLEAR is pressed.

Power-supply circuitry

The Stratix development board runs from a 9-V, unregulated, center-negative input. On-board circuitry generates 5-V, 3.3-V, and 1.5-V regulated power levels.

- The 1.5-V supply is used only for the Stratix device core power source and it is not available on any connector or header.
- The 3.3-V supply is used as the power source for all Stratix device I/O pins. The 3.3-V supply is also available to daughter cards or other devices plugged into any of the expansion connectors. The total load from all externally-connected 3.3-V devices may not exceed 500 mA.
- The 5-V supply is presented on pin 2 of JP12 for use by any devices plugged into the 5-V-tolerant expansion connectors. The total load may not exceed 50 mA.

Board Component List

See Table 2 on page 20 for a complete list of the Stratix development board components.

Figure 12. MJL Stratix Development Board Photo

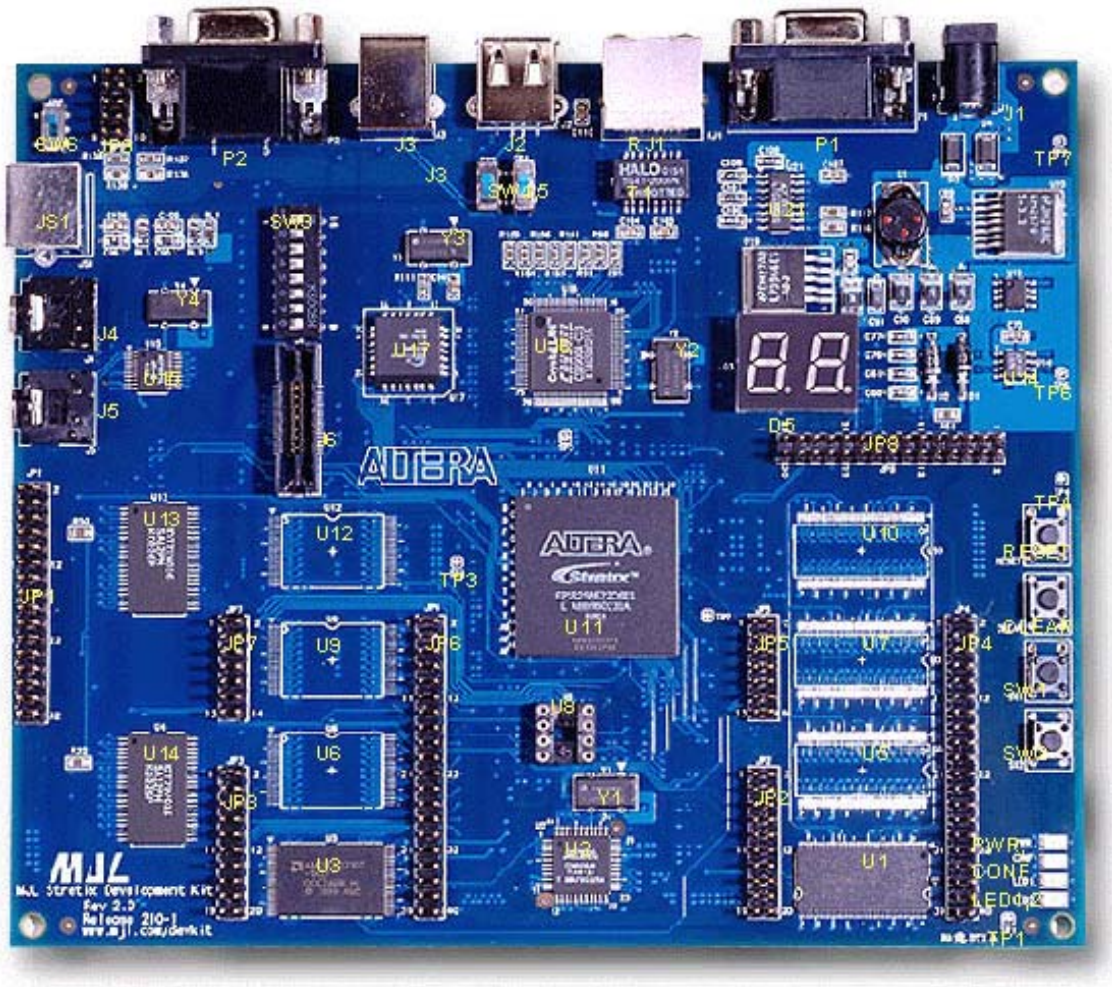


Table 2. Stratix Development Board Components (Part 1 of 2)	
D3	Dual-digit 7-segment LED
J1	Power supply connector
P1	Serial Port connector
SW6	Slide switch for configuration controller
JP9	JTAG header
JP4	40-pin header for 3.3 volt daughter card
JP5	14-pin header for 3.3 volt daughter card
JP2	20-pin header for 3.3 volt daughter card
JP6	40-pin header for 5 volt daughter card
JP7	14-pin header for 5 volt daughter card
JP3	20-pin header for 5 volt daughter card
LED1	User-controllable LED
LED2	User-controllable LED
CONF	Flash-byte LED
PWR	Power indication LED
SW3	8-bit DIP switch block
RESET	Resets the board-clears the Stratix device and reloads from the configuration controller
CLEAR	Clears the CPU
SW1	User-defined push-button
SW2	User-defined push-button
TP7	Ground point providing a ground plane reference
TP4	1.5 volt point providing a 1.5 volt plane reference
TP1	3.3 volt point providing a 3.3 volt plane reference
TP6	5 volt point providing a 5 volt plane reference
TP3	Main clock point
U11	Stratix EP1S25F672
U3	Flash memory device
U6	Flash memory device
U9	Flash memory device
U12	Flash memory device
U2	Stratix device configuration controller
U21	RS-232 level-shifter

Table 2. Stratix Development Board Components (Part 2 of 2)	
U13	SRAM
U14	SRAM
Y1	Programmable high-frequency oscillator(Main Clock)
Y3	USB oscillator
Y2	Ethernet oscillator
Y4	AD73311L oscillator
P2	VGA connector
JS1	PS2 connector
U15	AD73311L
J2	USB connector Type A
J3	USB connector Type B
SW4, SW5	Slide switch for the selection of USB Host/Slave
RJ1	Ethernet Connector
U14	Monitor Reset
U1	SDRAM
U5	SDRAM
U7	SDRAM
U10	SDRAM
J4	Microphone Jack
J5	Speaker Jack
J6	Mictor Connector
U17	USB Controller
JP8	30-pin header for free usage
JP1	23-pin header for free usage
U16	Ethernet Controller
T1	Transformer
U8	Oscillator Socket