Signal	Pin	Direction	Logic Level
sys_clk	N3	in	LVTTL
sys_res_n	AF17	in	LVTTL
btn_a	A3	in	LVTTL
btn_b	A5	in	LVTTL
led_a	A6	out	LVTTL
led_b	A7	out	LVTTL
uart_cts	D20	out	LVTTL
uart_rts	D21	in	LVTTL
uart_txd	D22	out	LVTTL
uart_rxd	D23	in	LVTTL
seg_1a	Y11	out	LVTTL
seg_1b	N7	out	LVTTL
seg_1c	N8	out	LVTTL
seg_1d	R4	out	LVTTL
seg_1e	R6	out	LVTTL
seg_1f	AA11	out	LVTTL
seg_1g	T2	out	LVTTL
seg_2a	R8	out	LVTTL
seg_2b	R9	out	LVTTL
seg_2c	R19	out	LVTTL
seg_2d	R20	out	LVTTL
seg_2e	R21	out	LVTTL
seg_2f	R22	out	LVTTL
seg_2g	R23	out	LVTTL
ps2_data	E21	bidirectional	LVTTL
ps2_clk	Y26	bidirectional	LVTTL
vga_r0	E22	out	LVTTL
vga_r1	T4	out	LVTTL
vga_r2	T7	out	LVTTL
vga_g0	E23	out	LVTTL
vga_g1	T5	out	LVTTL
vga_g2	T24	out	LVTTL
vga_b0	E24	out	LVTTL
vga_b1	T6	out	LVTTL
vga_hsync_n	F1	out	LVTTL
vga_vsync_n	F2	out	LVTTL