



Hardware Modeling



Hardware Description

ECS Group, TU Wien

Content of this course



- Hardware Specification
 - Functional specification
 - High Level Requirements
 - Detailed Design Description
 - Realisation
 - Hardware Description
 - Hardware Implementation
 - Verification
 - Review
 - Formal verification
 - Simulation
- 


Hardware Description: Outline



- ▶ Design entry
 - Levels of abstraction
 - Schematic entry vs. text-based entry

One possible method to describe hardware

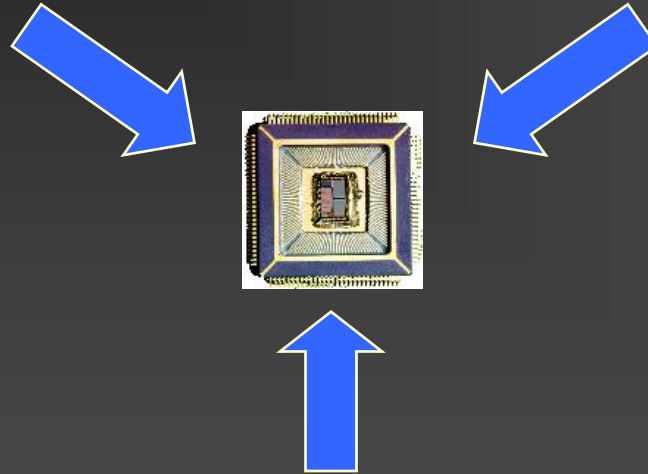


- ▶ VHDL
 - History
 - Motivation
 - Range of application
- 

Y-Diagram (1)

Behaviour of
the circuit

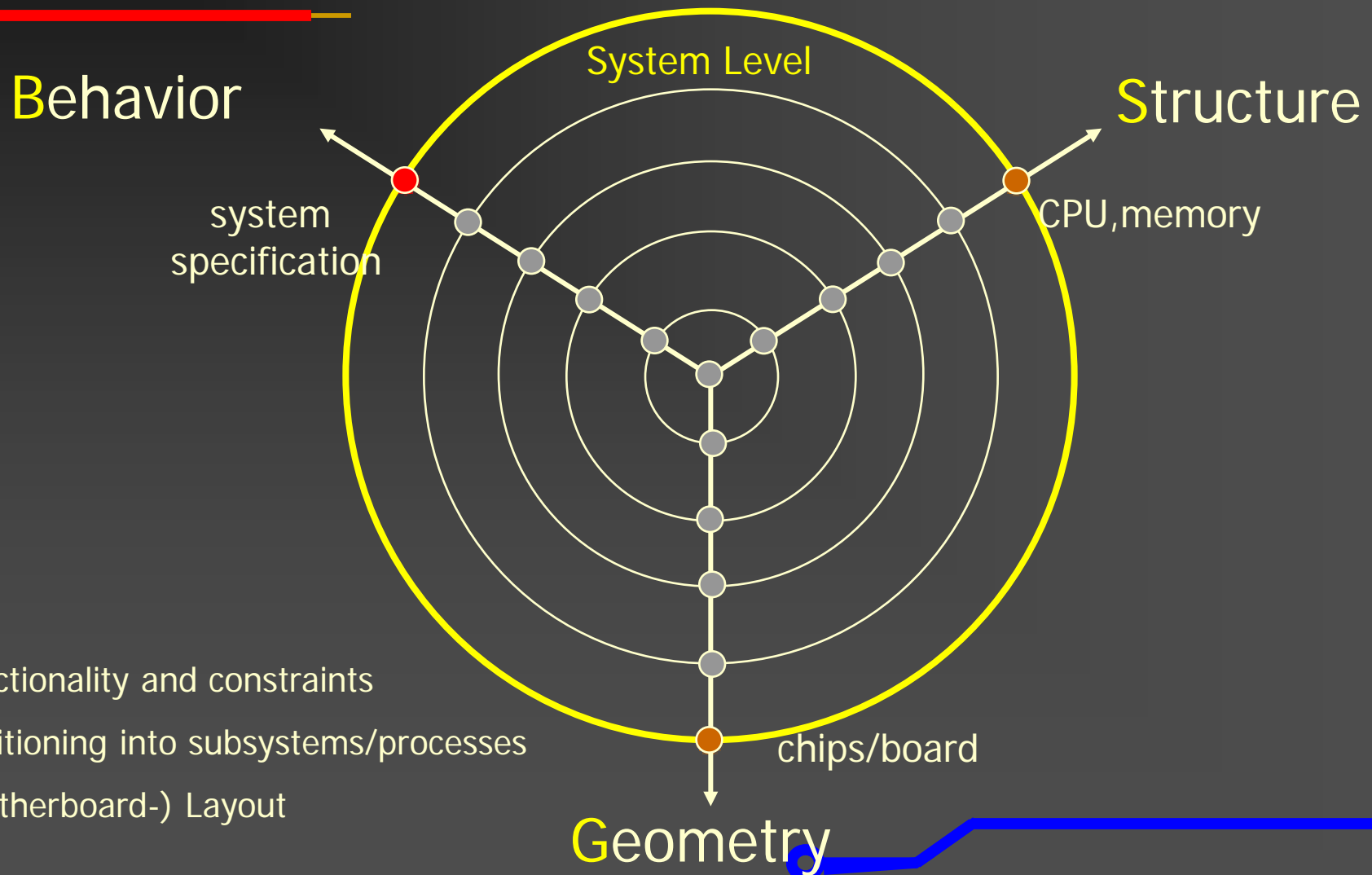
Components inside
the chip



Geometry of
the chip



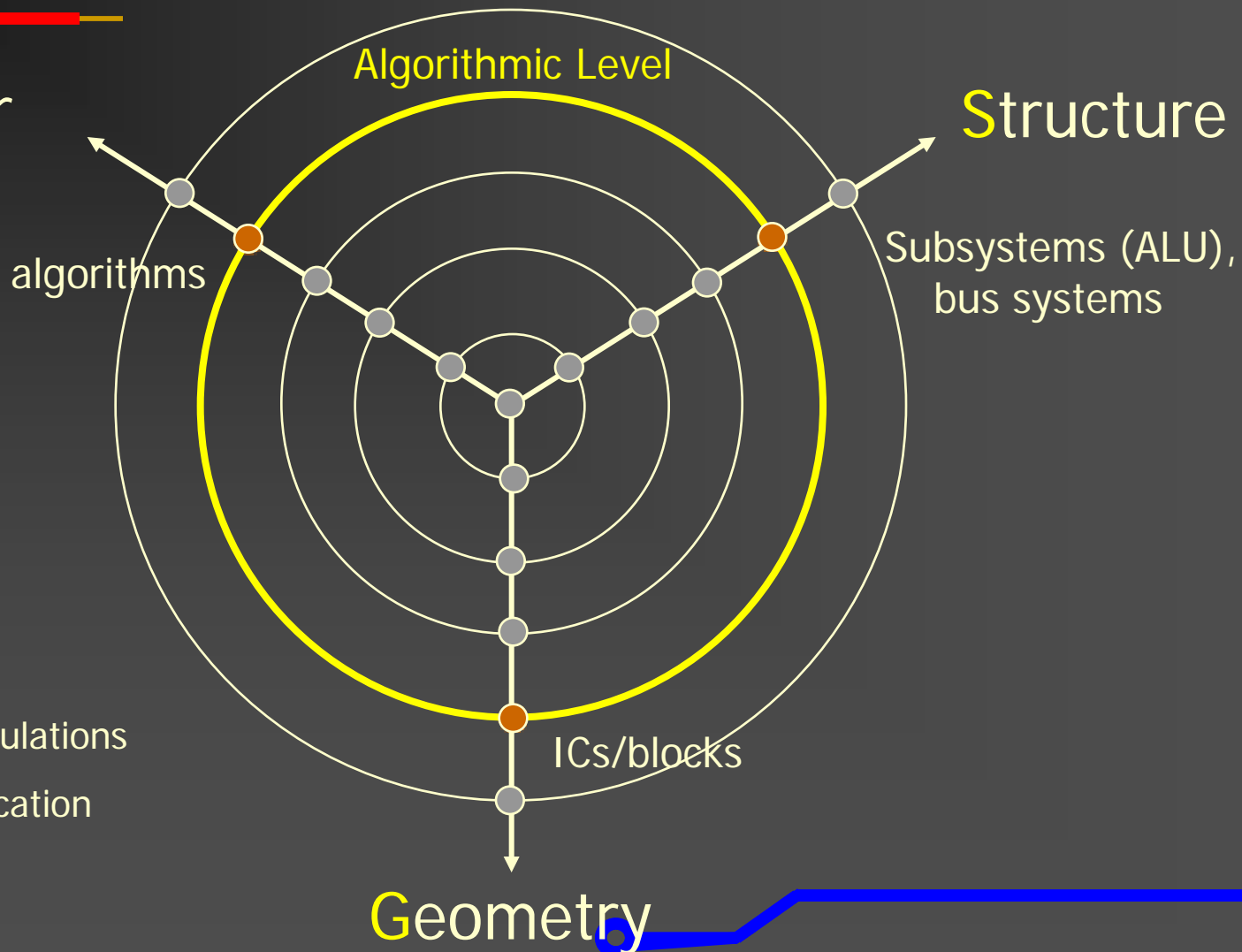
Y-Diagram (2)



- B: Functionality and constraints
- S: Partitioning into subsystems/processes
- G: (Motherboard-) Layout

Y-Diagram (3)

Behavior



Structure

algorithms

Subsystems (ALU),
bus systems

ICs/blocks

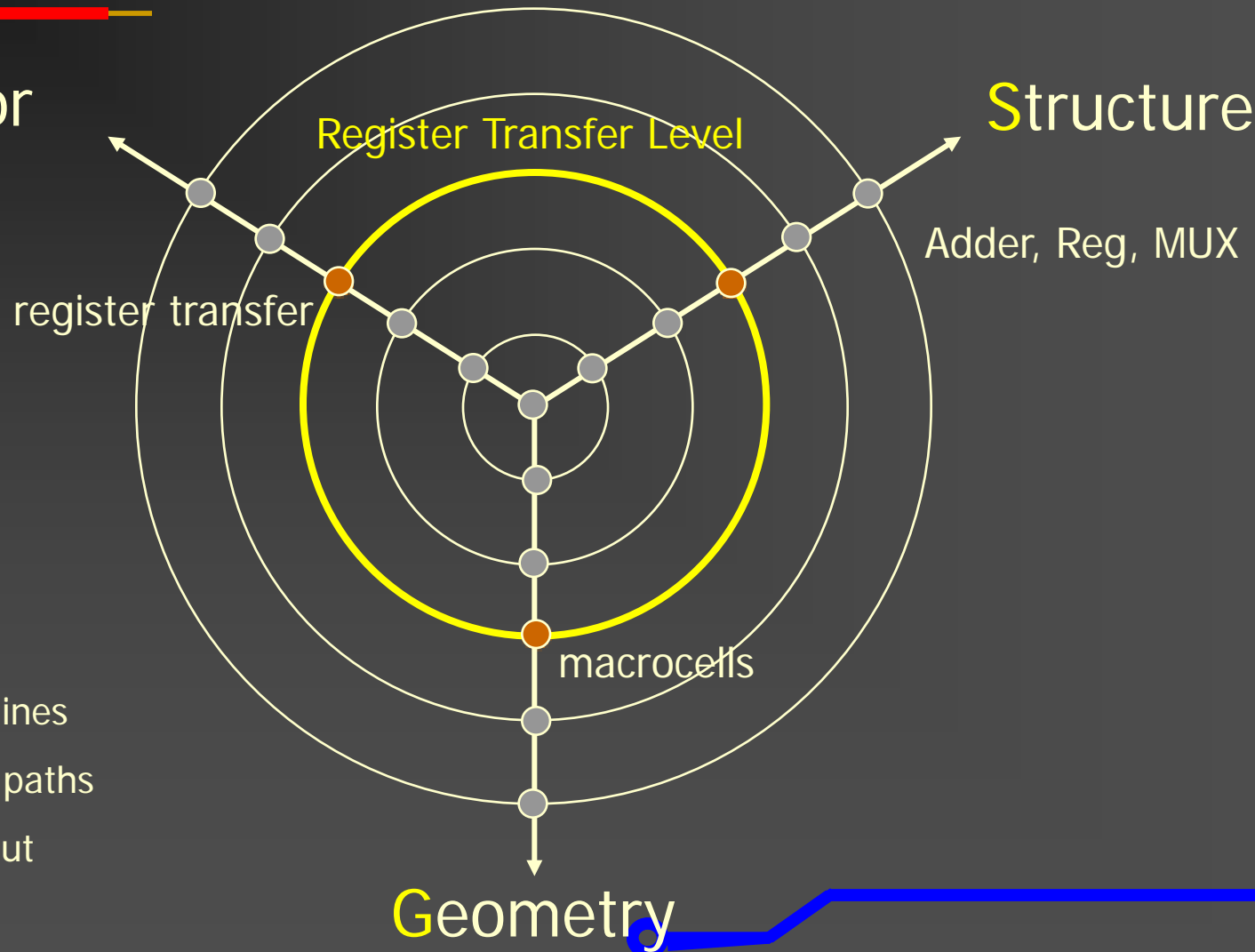
Geometry

- B: Operations and calculations
- S: Scheduling and allocation
- G: Chip-Layout

Y-Diagram (4)

Behavior

Structure

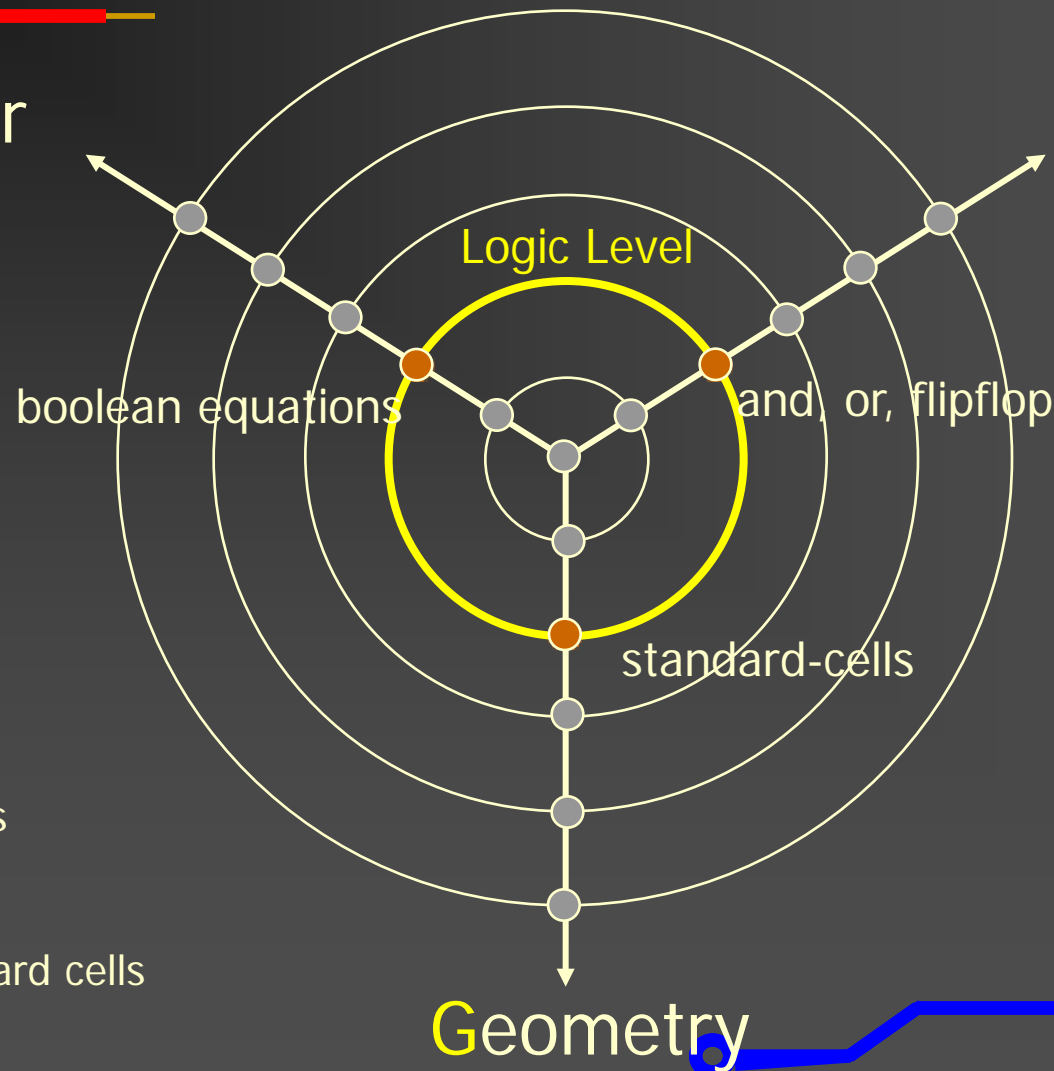


- B: Finite State Machines
- S: Data and control paths
- G: Refined chip layout

Y-Diagram (5)

Behavior

Structure



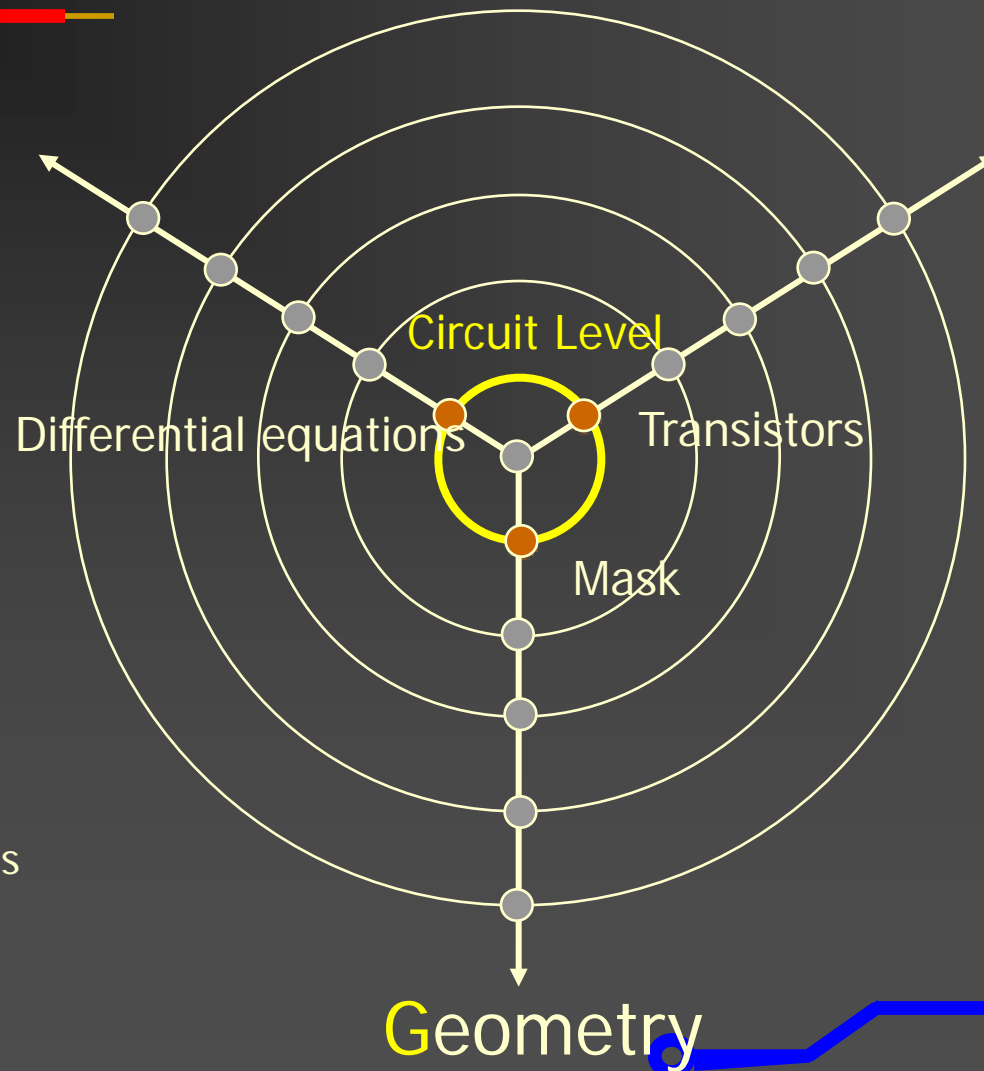
- B: Boolean functions
- S: Gate-level Netlist
- G: Position of standard cells

Geometry

Y-Diagram (6)

Behavior

Structure

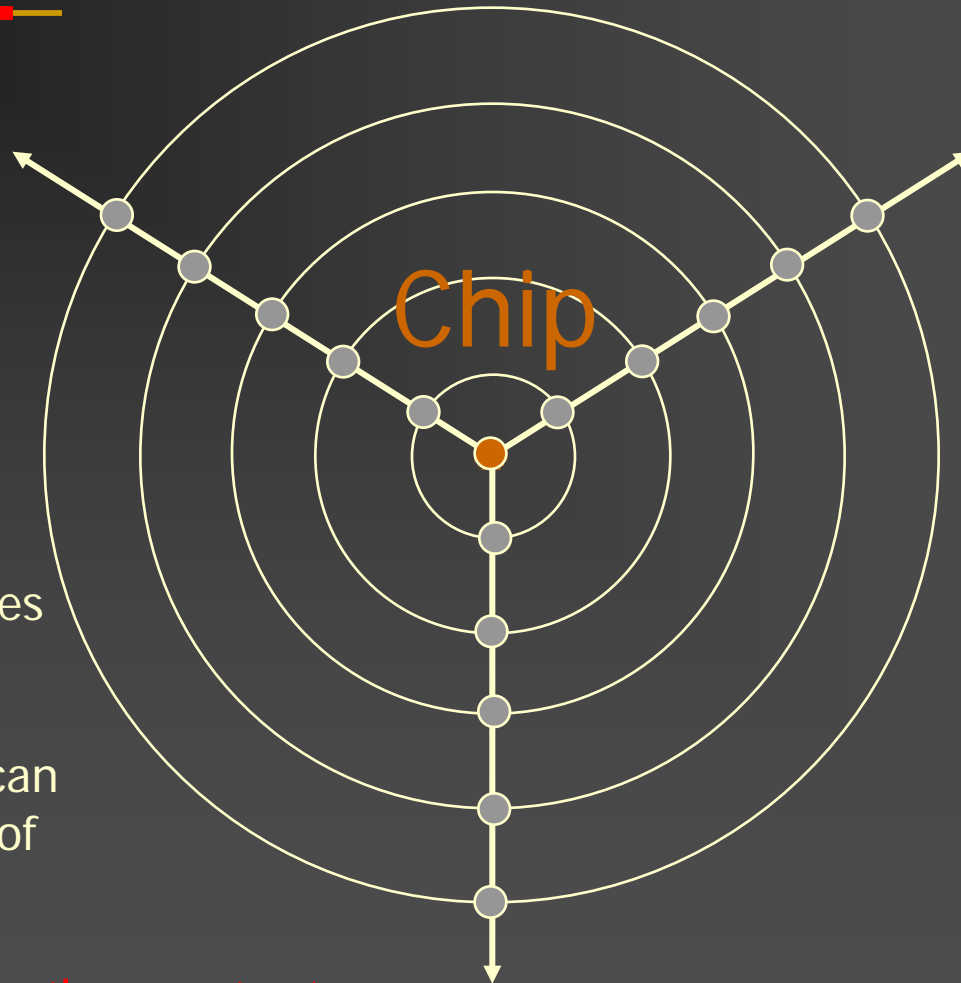


- **B:** Differential Equations
- **S:** Transistor network
- **G:** ASIC Mask

Y-Diagram (7)

Behavior

Structure



- The three views describes the **same** system/chip
- The **same** system/chip can be defined on all levels of abstraction

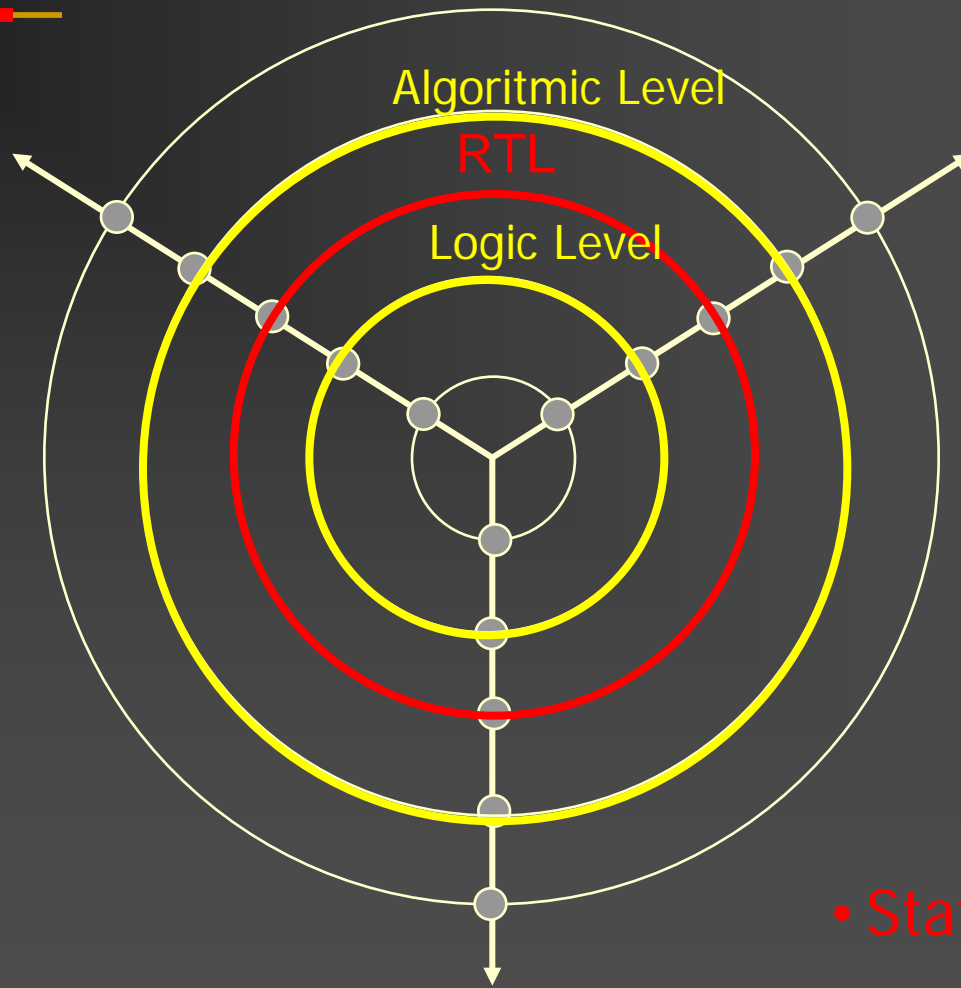
Geometry

⇒ Level of detail, information content

Hardware Description

Behavior

Structure

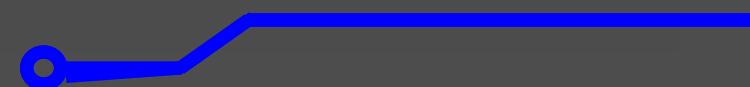


• State of the Art

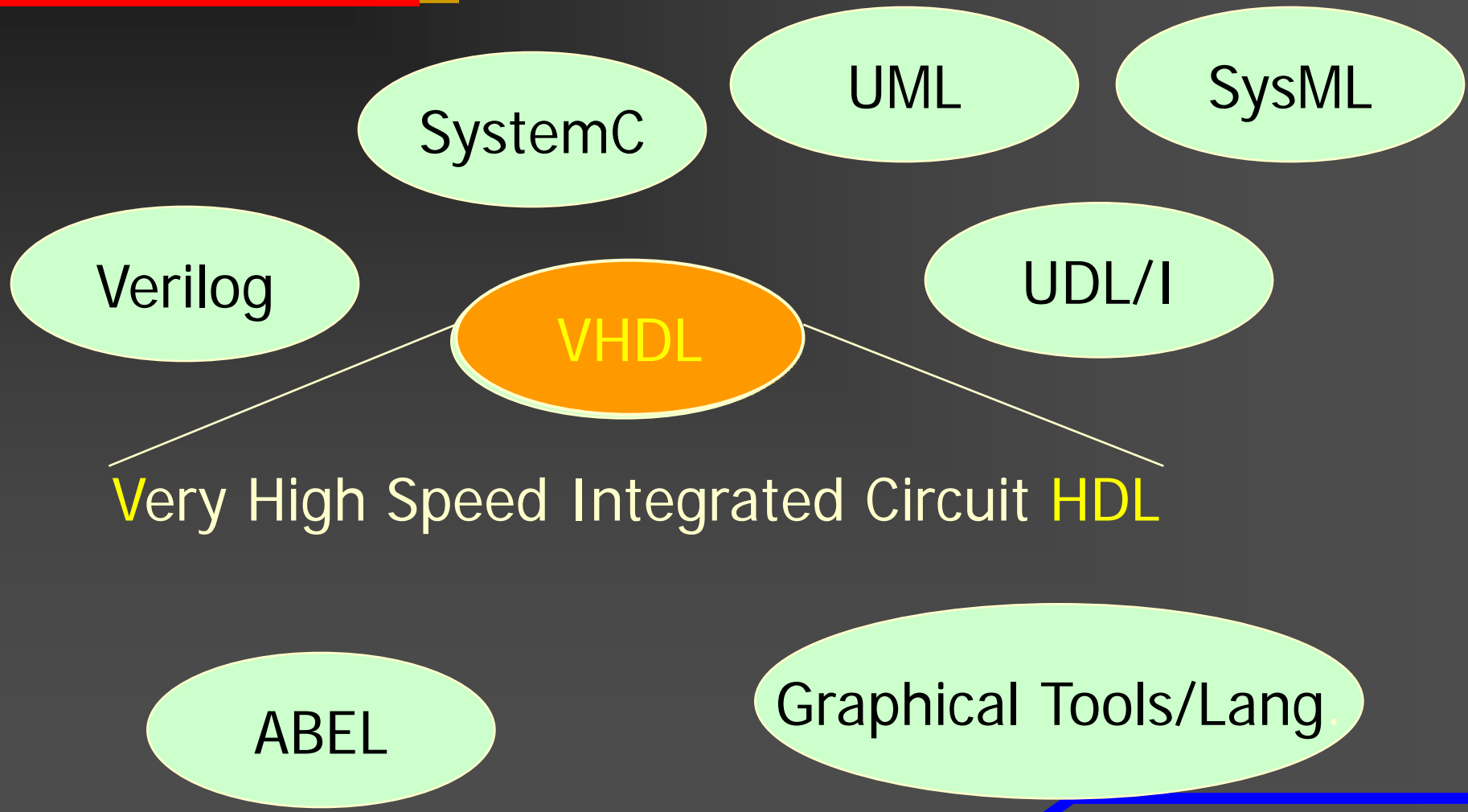
Geometry

Y-Table

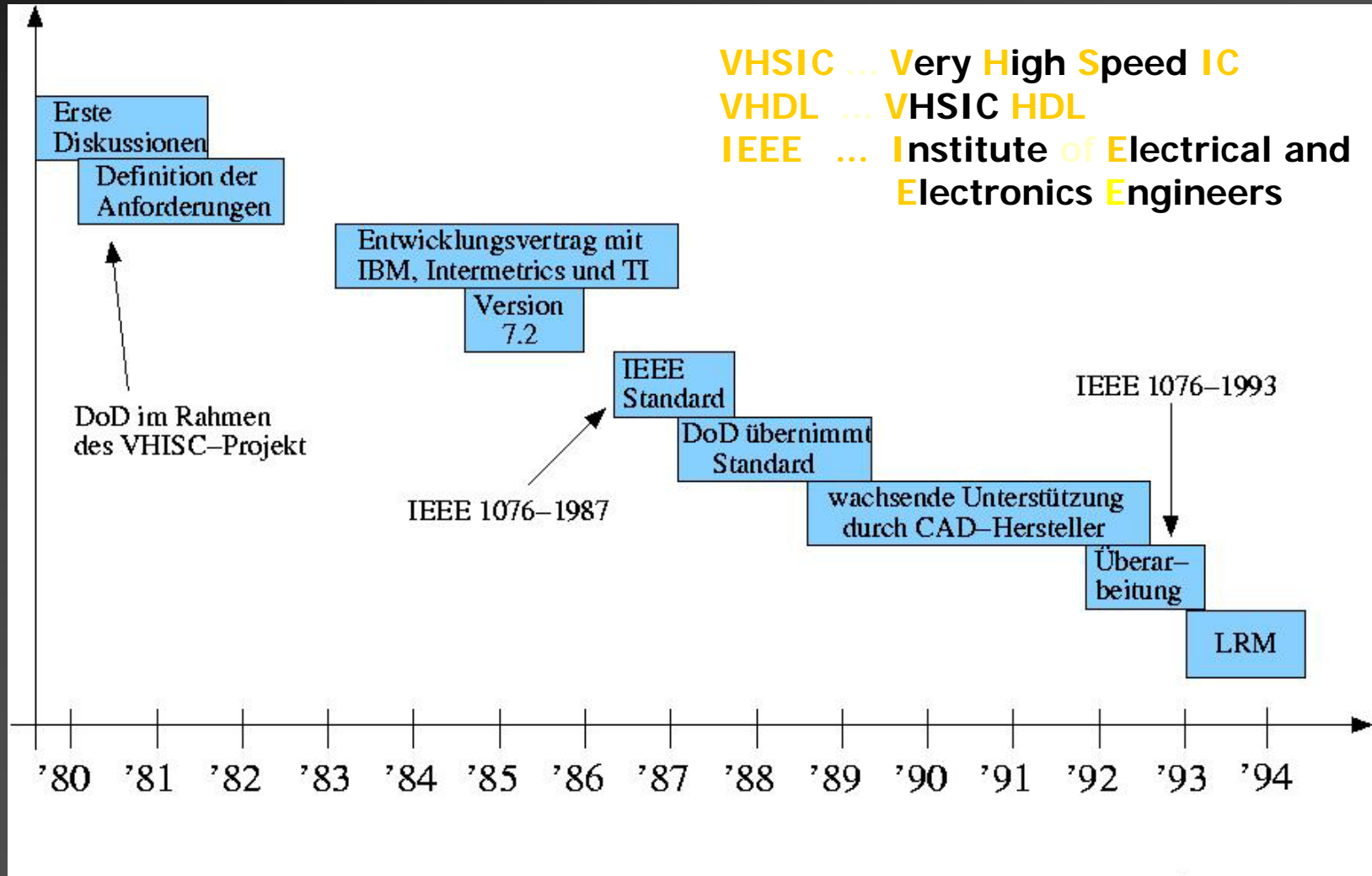
	Behavior	Structure	Geometry
System Level	<p>Inputs : Keyboard Output: Display Funktion:</p>		
Algorithmic Level	<pre>while input Read „Schilling“ Cal Euro Dis Euro</pre>		
Register Transfer Level (RTL)	<pre>if A = 1 then B := B + 1 else B := B end if</pre>		
Logic Level	<p>D = NOT E C = (D OR B) AND A</p>		
Circuit Level	$\frac{dU}{dt} = R \frac{dI}{dt} + \frac{1}{C} + L \frac{d^2I}{dt^2}$		



Hardware Description Languages




History of VHDL



Motivation: Documentation




Documentation for :

- Complex systems
 - Maintenance
 - Reusability
 - Different levels of abstraction
 - Readable man-machine interface
- 

Motivation: Data exchange



Data exchange between:

- Orderer and contractor
 - Developers
 - Tools
 - Computing systems
- 

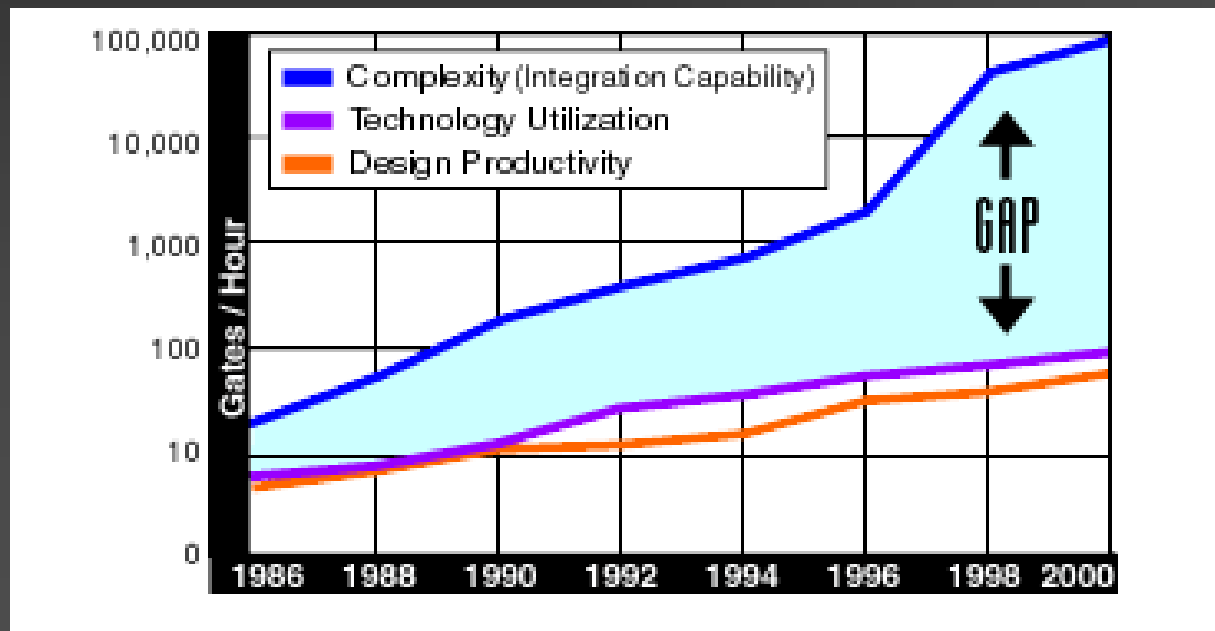
Motivation: Complexity (1)

Design Productivity Gap

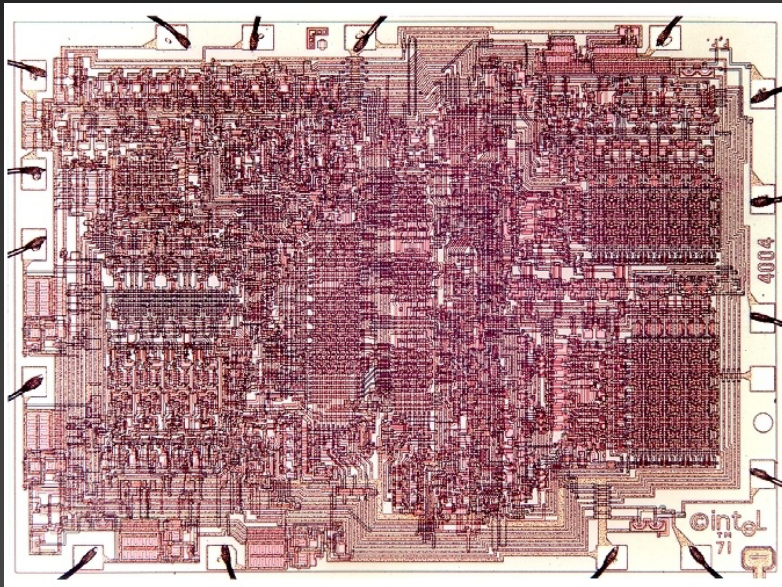
21%/Yr.
Productivity growth rate

VS.

58%/Yr.
Complexity growth rate

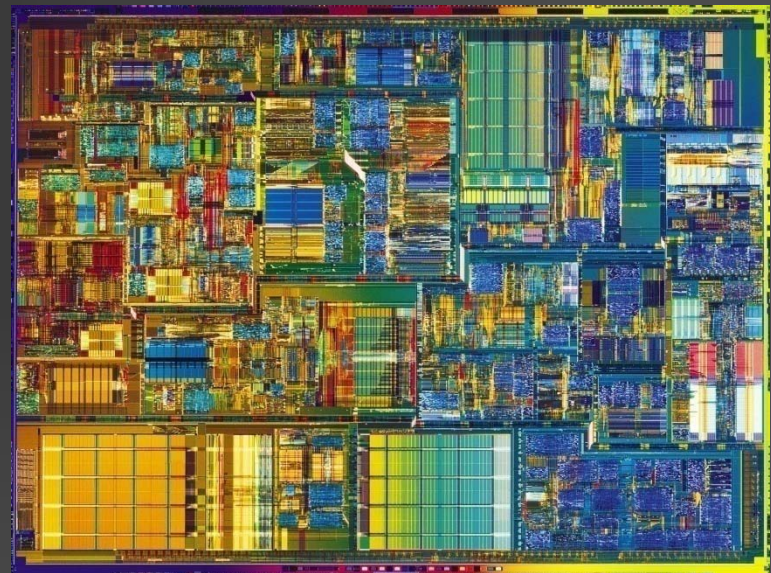


Motivation: Complexity (2)



Intel 4004 (1971)

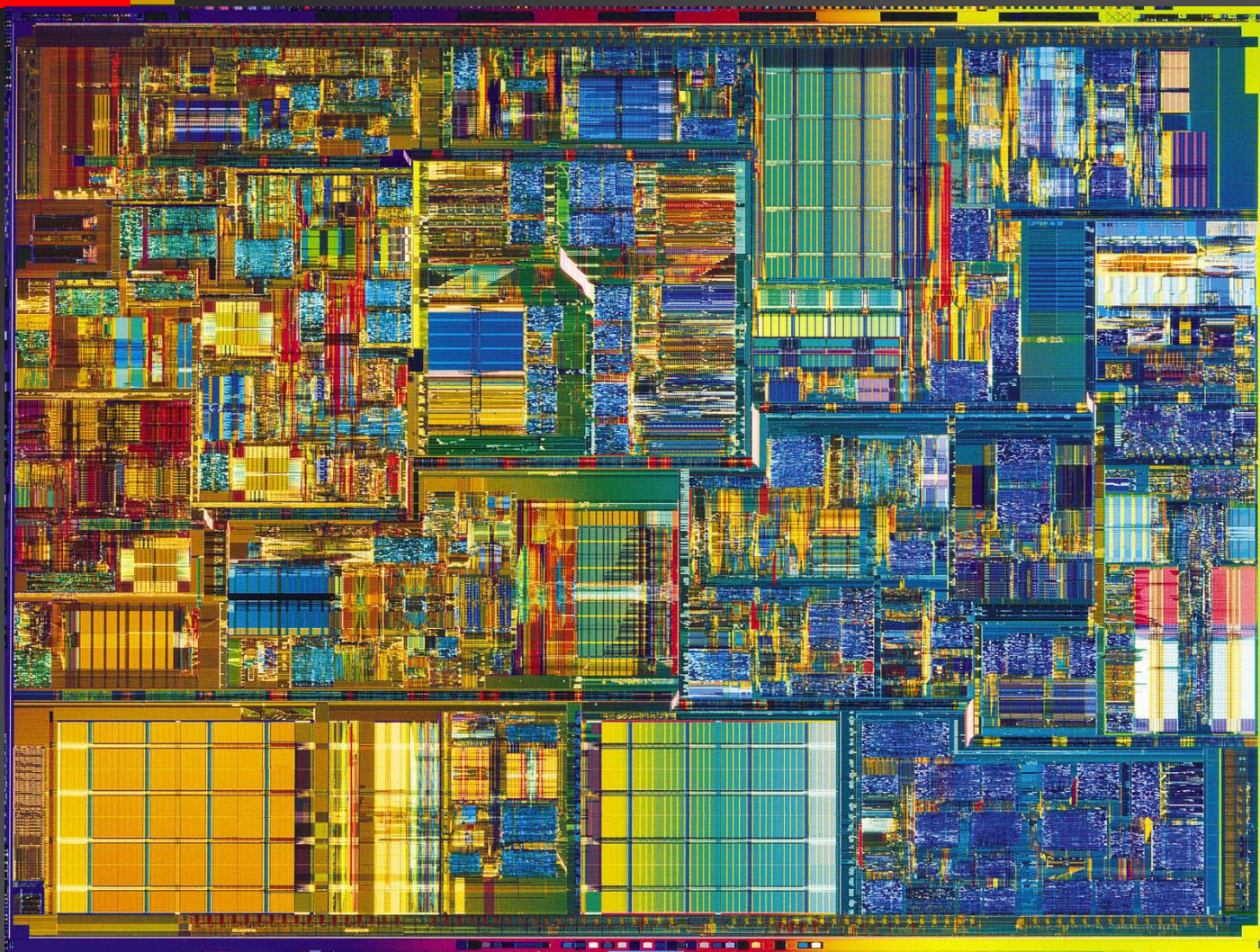
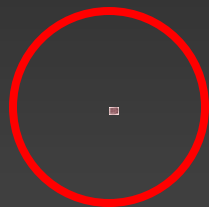
- 2300 Transistors
- 12 mm² / 10μm
- 108 kHz



Intel P4 (2001)

- 42 Millionen Transistors
- 217 mm² / 0,18μm
- 2 Ghz

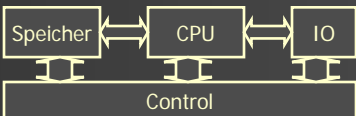

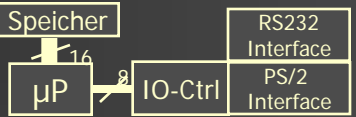


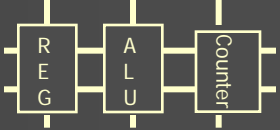
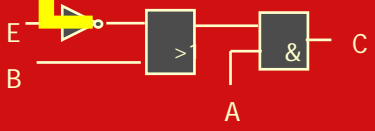
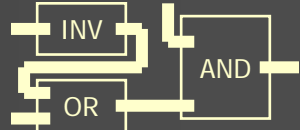
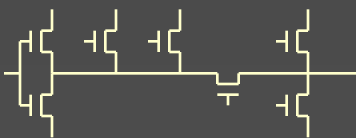

Motivation: Complexity (3)



Trans. count ratio:

1: 18261

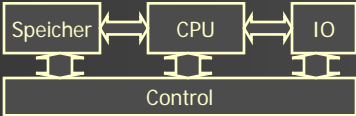

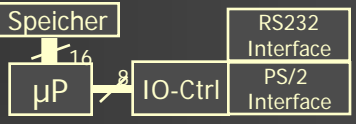


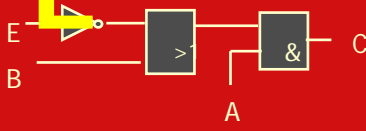
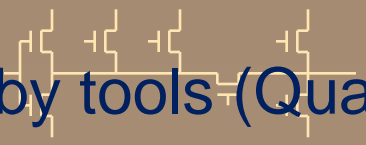
Range application of VHDL

	Behavior	Structure	Geometry
System Level	Inputs : Keyboard Output: Display Funktion:		
Algorithmic Level	<pre>while input Read „Schilling“ Calculate Euro Display „Euro“</pre>		
Register Transfer Level (RTL)	<pre>if A = '1' then B := B + 1 else B := B end if</pre>		
Logic Level	<pre>D = NOT E C = (D OR B) AND A</pre>		
Circuit Level	$\frac{dU}{dt} = R \frac{dI}{dt} + \frac{1}{C} + L \frac{d^2I}{dt^2}$		

Testbench (VHDL)

VHDL

Range application of VHDL

	Behavior	Structure	Geometry
System Level	Inputs : Keyboard Output: Display Funktion:		
Algorithmic Level	Testbench (VHDL) while input Read „Schilling“ Calculate Euro Display „Euro“		
Register Transfer Level (RTL)	if A = '1' then B := B + 1 else B := B end if		Generated by Tools (Synplify, Synopsys)
Logic Level	D = NOT E C = (D OR B) AND A		
Circuit Level	$\frac{dU}{dt} = R \frac{dI}{dt} + \frac{1}{C} \int I dt + L \frac{d^2I}{dt^2}$		Generated by tools (Quartus, e.g.)

VHDL

Summary

- Hardware can be described from different view: **Behavioral, Structural** and **Geometrical**
- Hardware can be described on different **Levels of Abstraction**
- VHDL is **one approach** to describe hardware on **RTL and Boolean Level**

