



Hardware Modelling



Introduction

Jakob Lechner, Thomas Polzer


Lecture Organisation

- ▶ Lecturer: Jakob Lechner, Thomas Polzer
- ▶ Email: {lechner, tpolzer}@ecs.tuwien.ac.at
- ▶ Location: EI8
- ▶ Time: Tue, 04.03. until Thu, 13.04.
 - Tuesday: 12:15 - 14:00
 - Thursday: 12:15 - 14:00



The Lecture



- ▶ Overview hardware modelling
 - ▶ In-depth discussion of selected chapters
 - VHDL
 - Design Styles
 - State Machines
 - Design Flow / Synthesis & Simulation
 - Writing Testbenches / Verification
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The Lab

▶ Task:

- Implement a calculator on an FPGA board
- Input: PS/2 Keyboard
- Output: VGA Monitor


▶ Learning targets:

- Systematic approach to HW modelling
- Detailed knowledge of VHDL & Tools
- Writing precise design specifications



The Lab



- ▶ Location:
 - Tilab Room 1: PC ti4 - ti9
see: <http://www.tilab.tuwien.ac.at/timetable.shtml>
 - At home (all tools are freely available)
 - ▶ Groups:
 - Groups of two
 - Name your preferred colleague at myTI
 - ▶ Weekly Q&A hours in the lab room:
 - Dates to be announced next week
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Schedule



▶ Write a design document

- High-level design description
- Detailed design description
- Submission deadline: Fri, 26.03. 23:59 (via MyTI)

▶ Peer-Review

- Evaluate the document of two other groups
- Submission deadline: Fri, 16.04. 23:59 (via MyTI)

▶ Final submission of the design document

- Submission deadline: Fri, 30.04. 23:59 (via MyTI)

▶ Implementation

- VHDL Entry / Simulation / Synthesis / Hardware Testing
- Submission deadline: Fri, 28.05. 23:59 (via MyTI)

Grading



- ▶ Design documents (30 %)
 - 1st and 2nd version will be graded (with emphasis on then final version)
 - Peer-Review
 - ▶ Oral exam (70 %)
 - Presentation of your solution
 - Some questions about the lecture's content
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